Claims

I Claim:

1. A vertical FET device comprising:

a body of semiconductor material comprising a first conductivity type, wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact;

a first trench formed in the body of semiconductor material and extending from the upper surface, wherein the first trench has a first width, a first depth from the upper surface, first sidewalls, and a first bottom surface;

a second trench formed within the first trench, wherein the second trench has a second width, a second depth from the first surface, second sidewalls and a second bottom surface, wherein the first and second trenches form a first trench structure;

a first source region formed in the body of semiconductor material extending from the upper surface and spaced apart from the first trench; and

a first doped gate region formed in at least a portion of the second sidewalls and the second bottom surface, wherein the doped gate region comprises a second conductivity type.

2. The device of claim 1 wherein the body of semiconductor material comprises a III-V semiconductor substrate having a first dopant concentration and a first epitaxial layer formed on a surface of the semiconductor substrate, wherein the first epitaxial layer has a second dopant concentration less than the first dopant concentration.

3. The device of claim 1 wherein the body of semiconductor material comprises one of GaAs and InP.

4. The device of claim 1 further comprising:

a first passivation layer formed over the doped gate region; and

a planarized passivation layer formed over the first passivation layer.

5. The device of claim 1 further comprising a second source region in the body of semiconductor material spaced apart from the first trench, wherein the first trench is between the first and second sources.

6. The device of claim 1 further comprising a gate coupling region formed in the body of semiconductor material, wherein the gate coupling region is connected to the first doped gate region.

7. The device of claim 1, wherein the vertical FET device comprises a depletion mode FET device.

8. The device of claim 7, wherein the depletion mode FET comprises an n-channel depletion mode FET device.

9. The device of claim 1 further comprising:

a second trench structure formed in the body of semiconductor material;

a second source region formed in the body of semiconductor material extending from the upper surface and spaced apart from the second trench structure;

a second doped gate region formed in the second trench structure;

a first source contact region coupled to the first source region;

a second source contact region electrically isolated from the first source contact region and coupled to the second source region;

a common drain region formed in the body of semiconductor material; and

a gate contact region coupled to the first and second doped gate regions.

10. A semiconductor switching structure comprising:

a depletion mode compound semiconductor sense FET device having a first gate region;

a depletion mode compound semiconductor main FET device having a second gate region;

a first source contact region coupled to the sense FET;

a second source contact region coupled to the main FET; and

a gate control pad coupled to the first and second gate regions.

11. The structure of claim 10 wherein the sense FET device comprises a vertical GaAs n-channel depletion mode FET device.

12. The structure of claim 10 wherein the main FET device comprises a vertical GaAs n-channel depletion mode FET device.

13. The structure of claim 10 wherein the main FET device and the sense FET device are formed within a common body of semiconductor material.

14. The structure of claim 10 wherein the main FET device comprises a vertical double trench FET.

15. The structure of claim 10 wherein the sense FET device comprises a vertical double trench FET.

16. The structure of claim 10 wherein the main FET device comprises:

a body of semiconductor material comprising a first conductivity type, wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact;

a first trench formed in the body of semiconductor material and extending from the upper surface, wherein the first trench has a first width, a first depth from the upper surface, first sidewalls, and a first bottom surface;

a second trench formed within the first trench, wherein the second trench has a second width, a second depth from the first surface, second sidewalls and a second bottom surface, wherein the first and second trenches form a first trench structure;

a first source region formed in the body of semiconductor material extending from the upper surface and spaced apart from the first trench; and

a first doped gate region formed in at least a portion of the second sidewalls and the second bottom surface, wherein the doped gate region comprises a second conductivity type.

17. A compound semiconductor vertical FET device comprising:

a first groove formed in a compound semiconductor layer of a first conductivity type, wherein the first groove has first sidewalls and a first lower surface, and wherein the first groove extends from a first surface of the compound semiconductor layer;

a second groove formed within the first groove, wherein the second groove has second sidewalls and a second lower surface;

a doped gate region formed in the second lower surface and at least a portion of the second sidewalls, wherein the doped gate region comprises a second conductivity type;

a first source region of the first conductivity type formed in the compound semiconductor layer adjacent to the first groove;

a source contact coupled to the first source region;

a gate contact coupled to the gate region; and

a drain contact formed on a second surface of the compound semiconductor layer.

18. The device of claim 17 wherein the body of compound semiconductor material comprises one of GaAs and InP.

19. The device of claim 17 wherein the vertical FET device forms an n-channel depletion mode sense FET.

20. The device of claim 17 wherein the vertical FET device forms an n-channel depletion mode power switching FET.